SYLLABUS

1. Course title:

Sequential Circuits

2. Code:

TK002

3. Cycle of study:

1

4. ECTS credits:

6

5. Type of course:

(•) Mandatory ( ) Elective

6. Prerequisites:

7. Class restrictions:

8. Duration / semester:

1 4

9. Weekly contact hours:

9.1. Lectures: 3

9.2. Seminars: 1

9.3. Laboratory/Practice classes: 1

10. Faculty:

Faculty of Electrical Engineering

11. Department/study program:

Electrical Engineering and Computer Science

12. Lecturer:

Assoc.Prof. Samra Mujačić, PhD

13. Lecturer's e-mail:

samra.mujacic@untz.ba

14. Web site:

15. Course aims:

The aim of this course is to teach students in the fundamental principles of digital systems analysis, design and synthesis, and to introduce VHDL language for digital systems design and synthesis.

16. Learning outcomes:

Students will be able to:
- Identify and analyze combinational circuits,
- Perform analyses and synthesis of sequential circuits,
- Understand the architecture and operations of a simple model of microprocessor.

17. Course content:

Introduction - digital logic and logic circuits. Combinational logic circuits and modular combinational logic. Latches and flip-flops. Synchronous sequential circuits. JEV-Mealy and Moore's machine. Analysis and synthesis of synchronous sequential circuits. Asynchronous sequential circuits. Sequential modules. Registers and counters. VHDL for combinational and sequential circuits. Digital systems design. Arithmetic and logic circuits. Memory structures. Basics of computer buses. Model of microprocessor.

18. Learning methods:

The most significant learning methods are as follow:
- Multimedia-based lectures and active learning techniques;
- Tutorials;
- Individual laboratory assignments.

19. Assessment methods:

First written assessment is to be delivered after half of the semester, which includes processed themes during the first part of the semester. Second written assessment is to be delivered at the end of the semester, which includes processed themes during the second part of the semester. The access to the second assessment is limited to the students who have passed the first one. Both assessment could be taken only once by the student. Students who do not pass those two assessments approach the final written exam, which carries the same points. As part of the pre-exam activities students are required to successfully complete all lab assignments. During the work in laboratory a teaching assistant assess the theoretical and practical knowledge of students. The final exam is oral for students who have passed both periodical assessments. The final exam is written and oral for students who have not passed the periodical assessments.
The results of continuous and final assessments are recognized as the passed exam if the cumulative result is achieved upon the positive verification of the individual assessment and is at least 50% of the scheduled and/or the required knowledge and skills.
In order for the student to pass the course he/she must achieve a minimum of 54 cumulative points.

20. Assessment components:

- I Continuous Assessment (55%)
  1. In-class attendance (5%)
  2.Periodical assessments (50%)
- II Final assessment (45%)

21. Required reading list:

- S. D. Brown, Z. G. Vranešić, Fundamentals of Digital Logic with VHDL Design, McGraw-Hill, 2009.
- S.Mujačić, Digitalni sistemi I, I dio, PrintCom Tuzla, 2009.
- U.Peruško, V.Glavinić, Digitalni sustavi, Školska knjiga, Zagreb, 2005

22. Web sources:

(max. 687 characters)

23. Applicable starting from the academic year:

2016/2017

24. Adopted in the Faculty/Academy session:

04.04.2016